A Subsidiary of Gould Inc.

S50240/S50241/S50242

TOP OCTAVE SYNTHESIZER

Features

- ☐ Single Power Supply
- ☐ Broad Supply Voltage Operating Range
- ☐ Low Power Dissipation
- ☐ High Output Drive Capability
- ☐ S50240 — 50% Output Duty Cycle
- ☐ S50241 — 30% Output Duty Cycle
- ☐ S50242 — 50% Output Duty Cycle

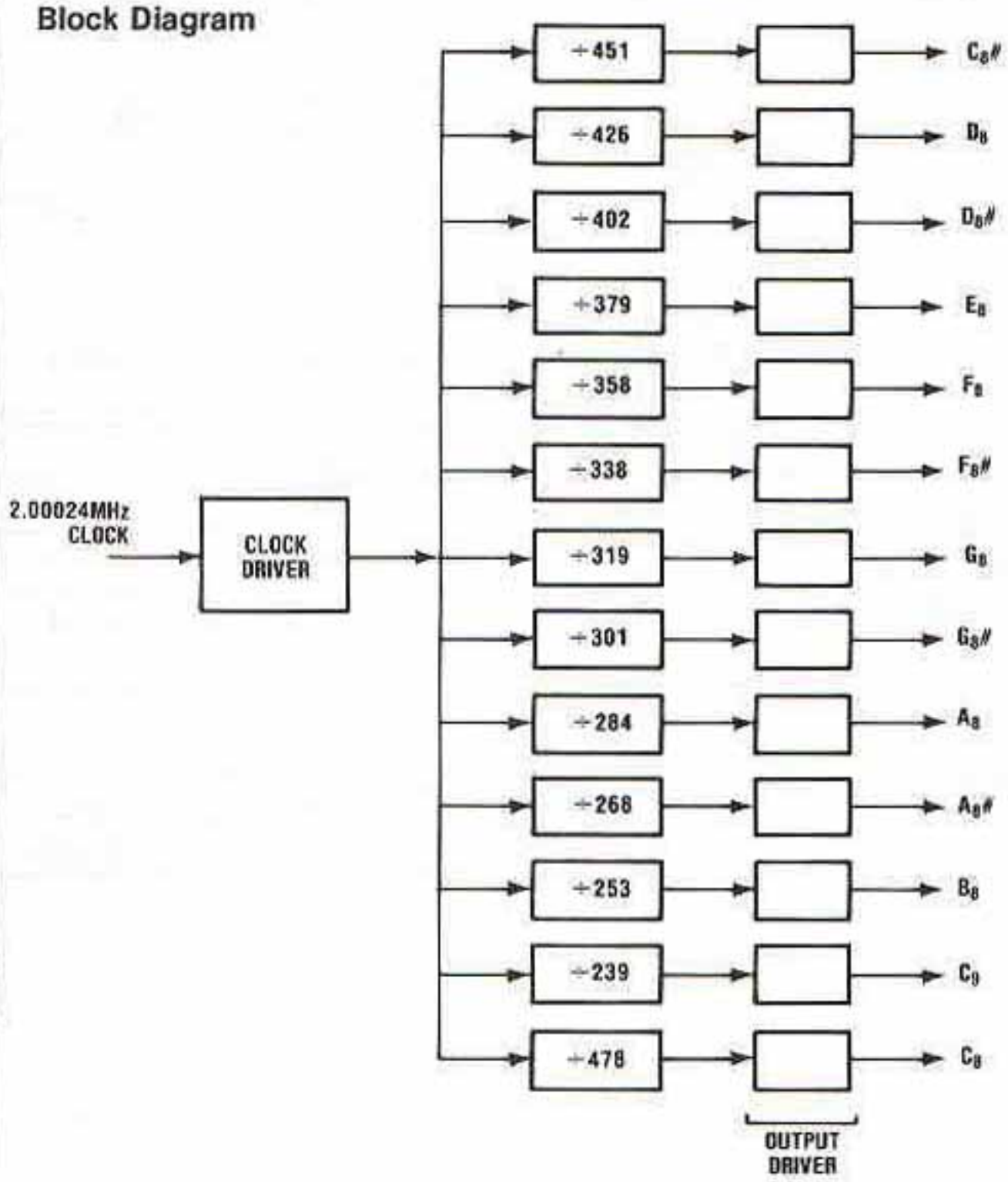
General Description

The S5024 is one of a family of ion-implanted, P-Channel MOS, synchronous frequency dividers.

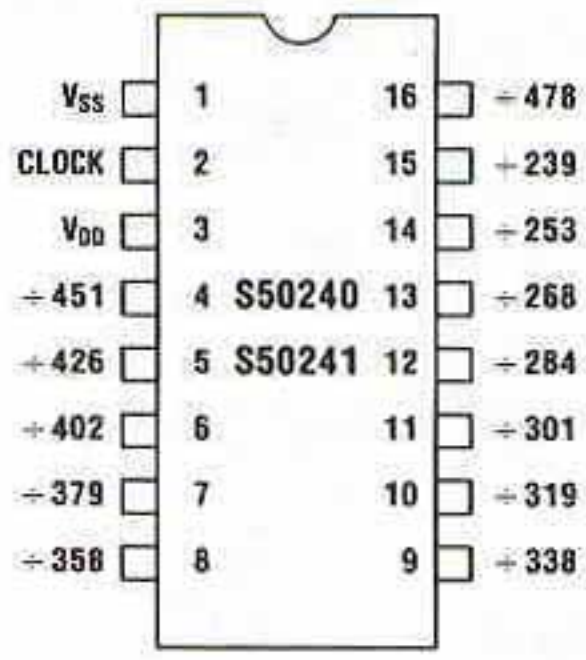
Each output frequency is related to the others by a multiple $12\sqrt{2}$ providing a full octave plus one note on the equal tempered scale.

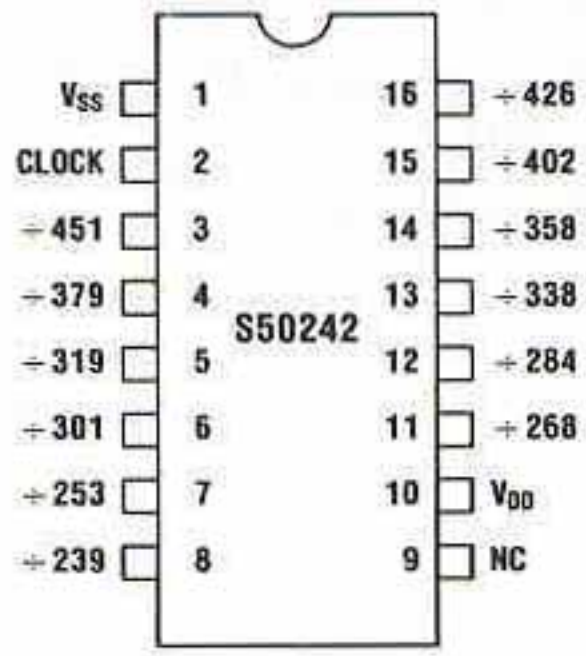
Low threshold voltage enhancement-mode, as well as depletion mode devices, are fabricated on the same chip allowing the S5024 family to operate from a single, wide tolerance supply. Depletion-mode technology also allows the entire circuit to operate on less than 360mW of power. The circuits are packaged in 16-pin plastic dual-in-line packages.

Block Diagram



Pin Connections





RFI emination and feed-through are minimized by placing the input clock between the V_{DD} and V_{SS} pins. Internally the layout of the chip isolates the output buffer circuitry from the divisor circuit clock lines. Also, the output buffers limit the minimum rise time under no load conditions to reduce the R.F. harmonic content of each output signal.

Absolute Maximum Ratings

Voltage On Any Pin Relative to V_{SS} ..... + 0.3V to − 20V
Operating Temperature (Ambient) ..... 0°C to 50°C
Storage Temperature (Ambient) ..... − 65°C to + 150°C

Recommended Operating Conditions ($0°C \leq T_A \leq 50°C$)

Symbol	Parameter	Min.	Typ.	Max.	Units	Figure
V_{SS}	Supply Voltage	0		0	V	
V_{DD}	Supply Voltage	−11.0	−14.0	−16.0	V	

Electrical Characteristics ($0°C \leq T_A \leq 50°C$; V_{DD} = − 11 to − 16V unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Figure
V_{IL}	Input Clock, Low	0		−1.0	V	Figure 1
V_{IH}	Input Clock, High	−10.0		V_{DD}	V	Figure 1
f_1	Input Clock Frequency	100	2000.240	2500	kHz	
t_r, t_f	Input Clock Rise and Fall Times 10% to 90% @ 2.5MHz			50	nsec	Figure 1
t_{ON}, t_{OFF}	Input Clock On and Off times @ 2.5MHz		200		nsec	Figure 1
C_I	Input Capacitance		5	10	pF	
V_{OH}	Output, High @ 1.0mA	V_{DD} + 1.5		V_{DD}	V	Figure 2
V_{OL}	Output, Low @ 1.0mA	V_{SS} − 1.0		V_{SS}	V	Figure 2
t_{ro}, t_{fo}	Output Rise and Fall Times, 500pF Load 10% to 90%	250		2500	nsec	Figure 3
t_{ON}	Output Duty Cycle—S50240, S50242 S50241		50 30		% %	
I_{DD}	Supply Current		14	22	mA	Outputs Unloaded

Figure 1. Input Clock Waveform

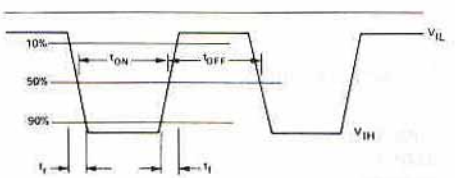


Figure 2. Output Signal DC Loading

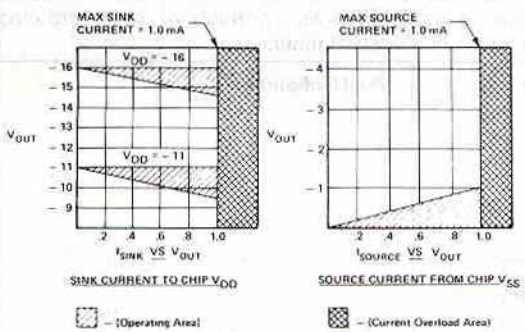


Figure 3. Output Rise and Fall Times